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Simulation of a 128-Bit Vedic Multiplier Integrated with Carry Look- Ahead Adder Using EDA Playground

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Abstract: *Multiplication is a fundamental operation in digital signal processing, cryptography, and scientific computing, where high precision and performance are critical. Traditional multiplication techniques become increasingly inefficient as operand sizes grow, especially in high-bit arithmetic. This paper presents an optimized design of a 128-bit Vedic multiplier based on the Urdhva Tiryakbhyam sutra, a fast and parallelizable multiplication algorithm derived from ancient Vedic mathematics. The proposed architecture decomposes the 128-bit operands into smaller segments, enabling concurrent partial product generation and reduction. This recursive and hierarchical approach significantly improves computation speed while maintaining low power and area footprints. The multiplier is implemented using a hierarchical approach to enhance speed and reduce area and power consumption. Simulated using EDA Playground, the proposed design demonstrates significant improvements in area, delay, and power compared to conventional multiplier architectures*

Keywords*:* Vedic Mathematics, Urdhva Tiryakbhyam, 128-bit Multiplier, EDA Playground, High-Speed Arithmetic, Low Power Design.

I. INTRODUCTION

In the realm of Very Large Scale Integration (VLSI) design, the need for high-speed and low- power arithmetic units is ever-growing. Multipliers, being integral components of digital systems, significantly influence the overall performance, area, and power consumption of processors, signal processing units, and cryptographic engines. As conventional multiplier architectures struggle to meet the dual demands of speed and efficiency at higher operand widths, alternative approaches have gained prominence.

Vedic Mathematics, a system derived from ancient Indian texts, introduces several arithmetic techniques that are algorithmically simple yet highly efficient. Among these, the Urdhva Tiryakbhyam Sutra—which means "vertically and crosswise"—has been recognized for its suitability in hardware implementations. This method facilitates parallel generation of partial products and concurrent addition, reducing the critical path delay and enabling faster computation.

Vedic multipliers have thus emerged as attractive alternatives in low-power VLSI systems, especially when implemented using advanced techniques such as pipelining, clock gating, and technology scaling. Their integration into standard-cell based ASIC and FPGA designs has demonstrated measurable improvements in area- delay-product and power-delay-product metrics.

This work focuses on designing an optimized 128-bit Vedic multiplier using the Urdhva Tiryakbhyam algorithm, implemented in 90nm CMOS technology. By exploiting the inherent parallelism and incorporating modern VLSI optimization strategies, the proposed design aims to deliver high computational throughput with reduced silicon footprint and power dissipation, making it ideal for integration in high- performance SoCs and embedded platforms.

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Vedic Mathematics and Urdhva Tiryagbhyam Sutra

The Urdhva Tiryagbhyam Sutra translates to "Vertically and crosswise" and is applicable to all cases of multiplication. It reduces partial product generation and enables parallelism, which is beneficial for high-speed hardware design.

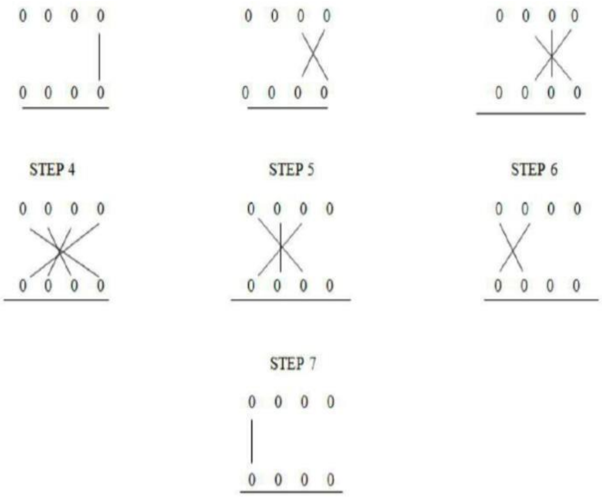

Figure 1: shows the multiplication of two 4-bit numbers using Urdhva Tiryagbhyam.

Carry Look-Ahead Adder (CLA)

CLA overcomes the delay in ripple-carry adders by computing carry signals in advance based on the inputs. The generate (G) and propagate (P) logic leads to faster computation of the carry chain:

- Generate: $G_i = A_i \cdot B_i$
- Propagate: $P_i = A_i \oplus B_i$
- Carry: $C_{i+1} = G_i + P_i \cdot C_i$

CLA is recursively used in our architecture to add partial products generated by the Vedic method.

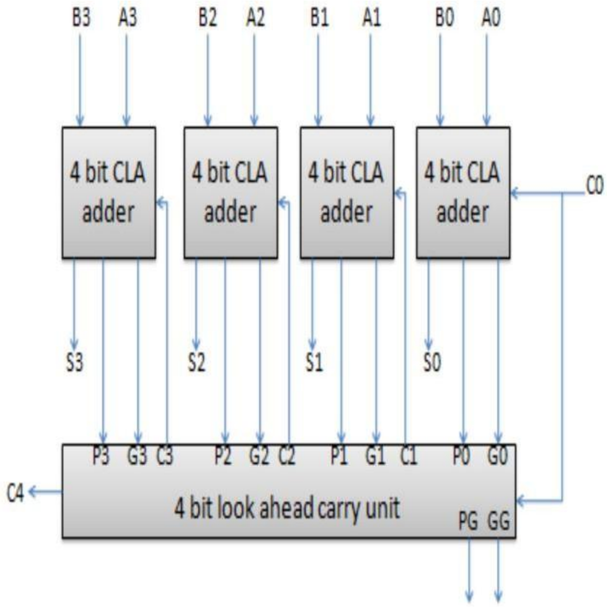

Figure 2: 4-bit CLA Architecture

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Vedic Multiplier with CLA

The block diagram description of a 128-bit Vedic Multiplier using Carry Look Ahead Adder (CLA). Since a 128-bit multiplier is too complex to design flatly, the proposed architecture recursively breaks down the 128-bit multiplication using smaller Vedic multipliers it is built hierarchically using smaller Vedic multipliers (e.g., 64-bit, 32-bit, 16-bit), and CLA adders are used for high-speed summation of partial products.

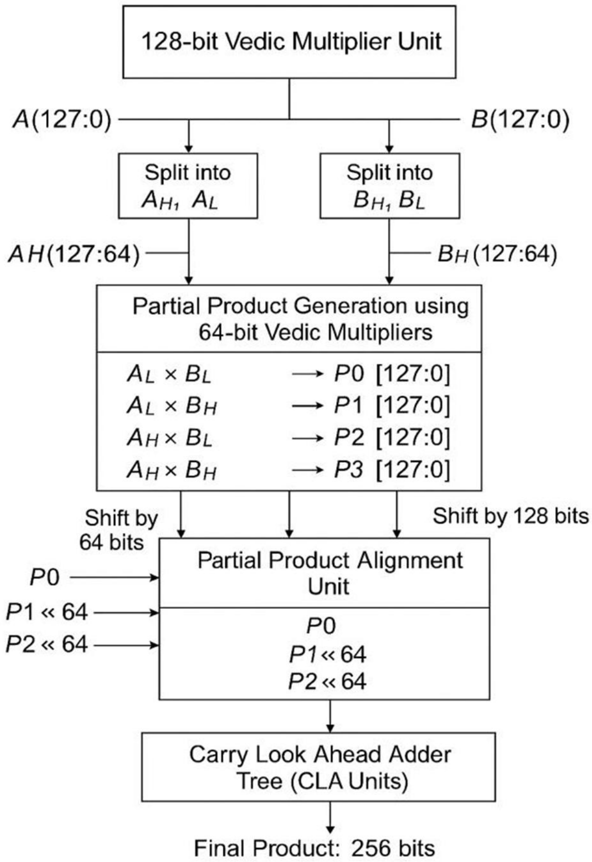

Figure 3: Block Diagram of 128-bit Vedic Multiplier using CLA

Block diagram of a 128-bit Vedic multiplier using Carry Look Ahead Adder. The 128-bit inputs are divided into 64-bit segments and processed through smaller Vedic multipliers. The resulting partial products are aligned through appropriate bit-shifting and summed using CLA adders to produce a high-speed 256-bit product.

Simulation Results

The design is simulated in EDA playground. The input-output waveforms of a 128 bit vedic multiplier are shown in Fig.4 A and B are the inputs and P is the output of the multiplier.

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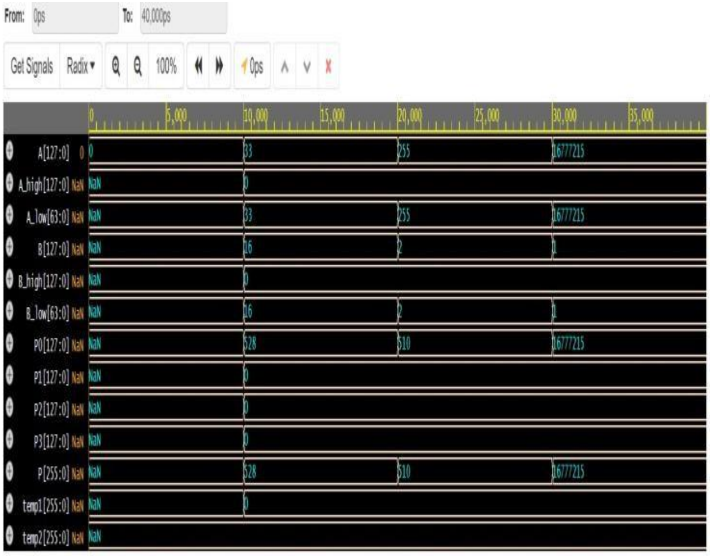

Figure 4: input and output waveform of 128 bit vedic multiplier

II. CONCLUSION

This paper demonstrates that combining Vedic multiplication with Carry Look-Ahead Adders provides a scalable, high-performance solution for large-bit-width multiplication. This approach is suitable for advanced VLSI systems, where speed and area are critical.

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