

Design of Advanced Multiplier using 15-4 Compressor

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Abstract: The major role of electronics device is to provide low power dissipation and compact area with high speed performance. Among the major modules in digital building blocks system, multiplier is the most complex one and main source of power dissipation. Approximate Computing to multiplier design plays major role in electronic applications, like multimedia by providing fastest result even though it possesses low reliability. In this paper, a design approach of 16 bit Wallace Tree approximate multiplier with 15-4 compressor is considered to provide more reliability. The 16×16 Wallace tree multiplier is synthesized and simulated using Xilinx ISE14.5 software. The multiplier occupies about 15% of total coverage area. The dissipated power and delay of the multiplier are 0.042μw, 3.125ns respectively.

Keywords: Kogge stone adder, 15-4 compressor, Wallace tree multiplier, area, power delay and Xilinx ISE14.5.

I. INTRODUCTION

Multipliers are the essential Part of the Digital system like Arithmetic and Logic Units, Digital Signal Processors, etc. Usually, they prompt the performance like power, delay and area utilization of the system. Hence there is an increasing demand for the improvement of performance of the multiplier [1-4]. The multiplier consists of 3 stages –partial products generation, partial products reduction and additional the last stage. The second stage (partial product) in multiplier utilize more time and power. Various techniques were suggested to diminish multipliers critical stages. The most popular technique is using the compressor in the reduction stage of partial product. The compressor is simply an adder circuit. It takes a number of qually-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number parallel manner. Their main application is within a multiplier, where partial products have to be summed up in a large amount concurrently. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values [5-7]. For the purpose of reducing the delay in the second stage, several compressors are needed. Small sizes of compressors are useful for designing the small size multiplier. In multiplier design, the different sizes of compressors are required depending upon the bit size. In this paper, a scheme for delay reduction in 16bitWallacetreemultiplierwith15:4compressor is considered. To build 15:4 compressor, a 5:3compressor is considered as a basic module. AND gate is used for the generation of partial products. For ‘N’ bit multiplier ‘N2’ AND gates are needed. In the partial product reduction phase, there are three major components namely half adder, full adder and 5-3 compressor [8-11]. The final stage of addition is done by using Kogge-Stone adder. Fig. 1 shows the structure of 16X16 multiplier. Simulation results show that the approximate multiplier with compressor using Kogge stone adder achieves high performance while comparing to the multipliers with compressor using other adder like parallel adder. This paper is elaborated in following sections. Designs of approximate 16×16 Wallace tree multiplier are detailed in section II. Brief notes and design of 15-4compressor, 5-3compressor and Kogge stone adder is described in section III. The section IV depicts the Result analysis. Section V concluded the overall paper.

II. WALLACE TREE MULTIPLIER

The three stages of Wallace tree multiplier are mentioned below:

1. Partial products generation
2. Partial products reduction
3. Addition at the final stage

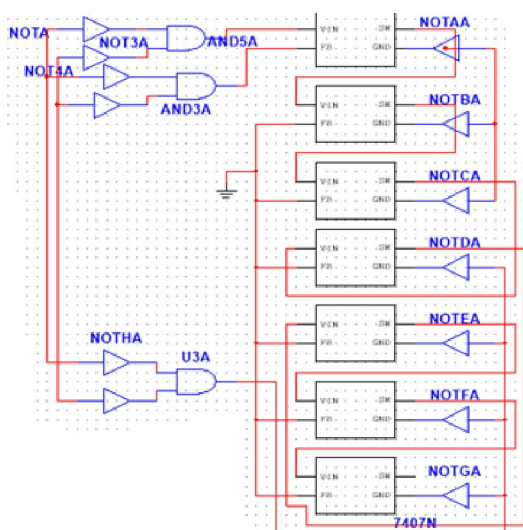


Fig. 1 and Fig. 2 describes the structure and schematic view of 16bit multiplier using with the help of 15-4 compressor.

Here in this design each dot denotes partial product. From 13th column onwards, 15-4 compressors are used in this multiplier architecture. Column number 13 consist of 13 partial products, in order to get 15 partial products 2 zeros are added. Similarly, in 14th column, one zero is added. Approximate compressors are used in 13th, 14th and 15th column of multipliers. The partial product reduction phase consists of half adder, full adder and 5:3 compressors. When the numbers of bits in the column are 2 and 3 half adders and full adders are used in each column. In case of a single bit, it is moved further to the subsequent level of that particular column without any need for further processing. Until only two rows will remain, this reduction process is repeated. Finally, summation of the last two rows is achieved using 4-bit Kogge-Stone adder.

III. 15-4 COMPRESSOR

A compressor is simply an adder circuit. It takes a number of equally-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. They are the important parts of the multiplier design as they highly influence the speed of the multiplier. Their main application is within a multiplier, where a huge number of partial products have to be summed up concurrently. For high speed applications like DSP, image processing needs several compressors to perform arithmetic operation. A compressor adder provides reduced delay over conventional adders using both half adders and full adders. Here the representation as 'N-r', in which 'N' denotes as the number of bits and 'r' denotes as the total number of 1's present in 'N' inputs. The compressor reduces the number of gates and the delay with reference to other adder circuits. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values. Compressors are widely used in the reduction stage of a multiplier to accumulate partial products in a concurrent manner. In this part it is considered the design of 15-4 compressor by using with approximate 5-3 compressors [5]. This compressor compresses 15 inputs (C0- C14) into 4 outputs (B0-B3). The 15-4 compressor consists of three phases. The first phase has five full adders, the second phase uses two 5-3 compressors and finally the 4-bit kogge stone adder. In this compressor design, approximate 5-3 compressor are preferred over accurate 5-3 compressors as shown in the Fig. 3

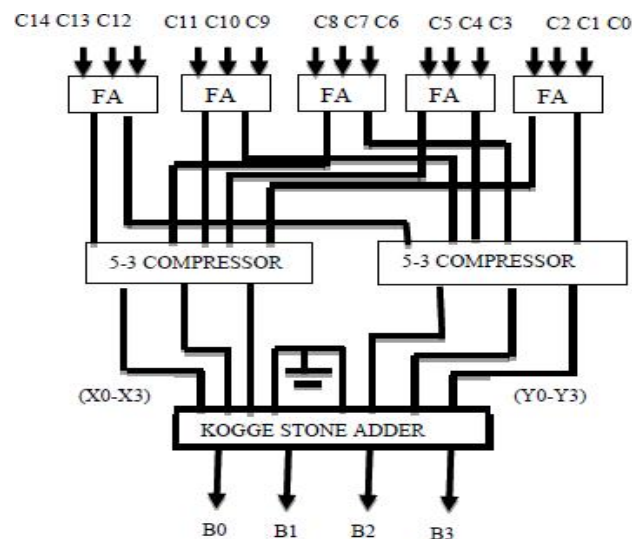


Fig. 3. Logic Diagram of Approximate 15-4 Compressor [6]

3.1 5-3 Compressor

The 15-4 compressor consists of 5-3 compressor as a basic design. The 5-3 compressor utilizes five primary inputs namely A0, A1, A2, A3, A4 and produces three outputs namely B0, B1, B2. In this compressor, the presence of number of 1's at the input decides the output of compressor and also uses counter property.

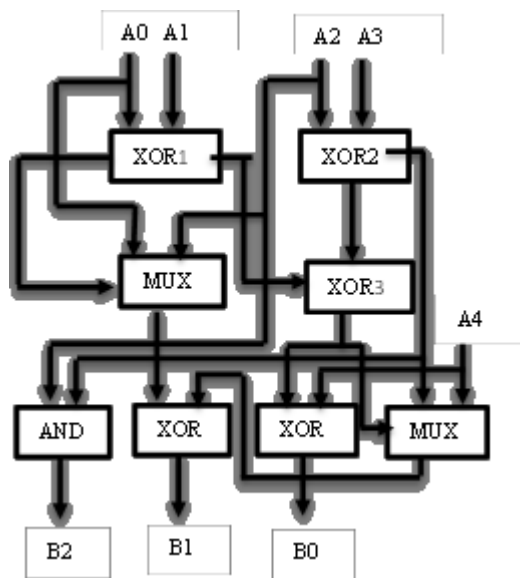


Fig.4. Logic diagram of 5-3 compressor

The design of compression of given 5 inputs into 3 output is called the design of 5-3 compressor. Error rate of 5-3 compressor is considered. The design equations of 5-3 approximate compressor are shown in following equations respectively. The logic diagram of approximate 5-3 compressor.

$$B_2' = [A_2, A_2]$$

$$B_2 = A_0 \cdot [\sim(A_0 \oplus A_1)] + A_2 \cdot (A_0 \oplus A_1) [A_2 \cdot (\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))] + A_4 \cdot [A_0 \oplus A_1 \oplus A_2 \oplus A_3]$$

$$B_1 = A_0 \cdot [\sim(A_0 \oplus A_1)] + A_2 \cdot (A_0 \oplus A_1) \oplus [A_2 \cdot (\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))] + A_4 \cdot [A_0 \oplus A_1 \oplus A_2 \oplus A_3]$$

$$B_0 = [A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4]$$

3.2 Kogge Stone Adder

In 1973, Peter M. Kogge and Harold S. Stone presented the idea of productive and superior adder called kogge-stone adder. It is essentially an equal prefix viper. This sort of adder has the forte of quickest expansion dependent on configuration time. It is known for its uncommon and quickest expansion dependent on configuration time [9], In Fig 5, shows the kogge stone adder Prefix Adders are for the most part characterized into 3 classes

A. Pre-Processing: In this stage, generate and propagate signals are given by the equations.

$$P_i = A_i \oplus B_i \quad G_i = A_i \cdot B_i$$

B. Generation of carry: In this stage, carries are calculated with their corresponding bits and this operation is executed in parallel manner. Carry propagation and generation are used as intermediate signals. The logic equations for carry propagate and generate are shown below.

$$G_i = (P_i \cdot G_{i-1}) + G_i$$

C. Final Processing: In final processing, the sum and carry outputs bits are computed for the given input bits and the logic equation for the final processing stage is given by

$$C_i = G_i$$

$$S_i = P_i \oplus C_{i-1}$$

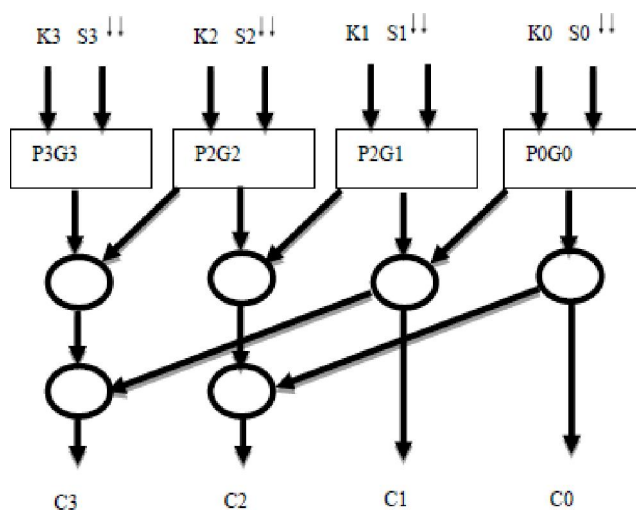


Fig 5: Block Diagram of Kogge Stone Adder

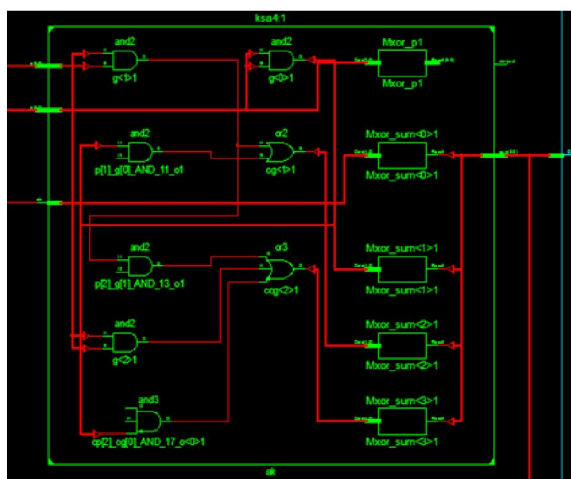


Fig.6. RTL view of kogge-stone adder

IV. SIMULATION RESULT

The design of approximate 16 bit Wallace multiplier using 15-4 compressor has been done in HDL, using Xilinx ISE 14.5. Simulation results show the design of overall architecture of Wallace tree multiplier as shown in Fig. 7. The parameters of area reutilized by the multiplier design and power consumption are obtained through simulation and tabulated in Table I and Table II. The snapshot of delay obtained through simulation is shown in Fig. 8. The processing delay at the end of addition level can be reduced by using kogges tone adder.

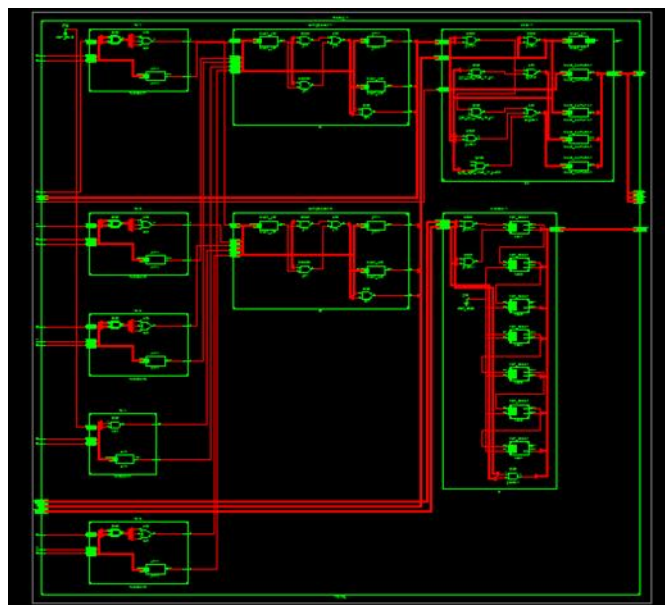


Fig.7.Overall Architecture Of 16×16 Bit Wallace Tree Multiplier

Table I and II describes the area utilization and power parameters of a 16-bit Wallace multiplier. It shows better result than other adder apart from that it gives less area and low propagation delay.

TABLE 1: DEVICE UTILIZATION OF 16×16 WALLACE TREE MULTIPLIER

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	20	63400	0%
Number of fully used LUT-FF pairs	0	20	0%
Number of bonded IOBs	33	210	15%

TABLE II: POWER ANALYSIS OF 16×16 WALLACE TREE MULTIPLIER

On-Chip	Power (W)
Logic	0.000
Signals	0.000
IOs	0.000
Leakage	0.042
Total	0.042

Timing Summary:

Speed Grade: -2

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 3.125ns

Fig.8.Delay analysis of 16×16 bit Wallacetree multiplier

TABLE III: DESIGN ANALYSIS OF MULTIPLIER

Sl.NO	Types of Multiplier	Area(μm^2)	Power(μw)	Delay(ns)
1	16×16 bit multiplier using Accurate 15-4 compressor	5066.2	563.20	4.24
2	16×16 bit multiplier using 15-4 compressor with 4-bit parallel adder	5159.3	557.2	4.24
3	16×16 bit multiplier using 15-4 compressor with kogge stone adder	1570	420	3.125

The performance of 15-4 compressor based approximate 16×16 multiplier is also compared with various adders at the final stage instead of Kogge stone adder. The comparative results in terms of reduced delay, area and power dissipation are tabulated in Table III.

V. CONCLUSION

The approximate 16×16bit Wallace tree multiplier using 15-4 compressor architecture has been designed and synthesized using on Spartan 3 XC3S100E board and simulated in XilinxISE 14.5. The performance of proposed Multiplier with kogge stone adder is compared with the same architecture of multiplier using parallel adder. It can be inferred that 16×16 multiplier architecture using 15-4 compressor with kogge stone adder is faster compared to multiplier with parallel adder. In future the performance of the proposed multiplier can be improved and applied in applications like video and image processing.

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